UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,984	12/11/2003	Hui-Min Mao	10113311	2073

34283 7590 09/19/2007

QUINTERO LAW OFFICE, PC
2210 MAIN STREET, SUITE 200
SANTA MONICA, CA 90405

EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
3663	

MAIL DATE	DELIVERY MODE
09/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,984	MAO ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-26 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-26 and 28-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 7/9/07 forms the basis for this Office Action. In said Amendment applicants substantially amended claims 23-26, and added four (4) new claims 28-31. Applicants cancelled claim 27 (not "withdrawn from consideration" as erroneously mentioned in Remarks). Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. ***Claims 23-24 and 28-29*** are rejected under 35 U.S.C. 102(b) as being anticipated by Chen (5,895,961).

On claim 23 and 28: Chen teaches a structure for a bit line contact hole (see contact hole with contact plug 48 as described below contacting source/drain region of the transistor with Poly 14a, hence bit line contact) comprising:

a substrate 10 (col. 4, l. 11);

a transistor (any of the transistors in the self-aligned transistor structure (col. 4, l. 6-19) disposed on the substrate, comprising a gate layer (14a or 14b) (col. 4, l. 11-19) covered by a first insulating layer (16a or 16b) (col. 4, l. 11-19) and comprising first and

second doped regions (source and drain regions using self-aligned process, hence necessarily on the sides of said gate layer) (col. 4, l. 20-28);

an inner landing pad (either 20/22 or 22) disposed on the first doped region (between poly 14a and poly 14b) (Fig. 17 and col. 4, l. 28-40), disposed on the first doped region (centered between 14a and 14b), comprising a polysilicon layer 22 (loc.cit.);

a passivation layer 26 capable of serving as a diffusion barrier by virtue of being a massive insulating oxide (col. 4, l. 50-51), formed on the inner landing pad, the transistor and the substrate (see Figure 17), wherein the passivation layer is in contact with the second doped region (to the left of Poly 14a) (see Figure 17);

a second insulating layer comprising doped materials (BPSG) (col. 4, l. 50-55 and Figure 17), disposed on the passivation layer, having a flat surface on the passivation layer (see Figure 17);

a contact plug (central portion of 48a directly above Poly 14a: see Figure 17), disposed on the second insulating layer and the passivation layer, electrically connected with the inner landing pad (by abutting 22), and

an interconnected landing pad (wider upper portion with wing portions on both sides of said central portion of 48a (see Figure 17)), deposited on the central portion (loc.cit.).

In connection with the limitation "serving a barrier layer" only the capability to serve a barrier layer carries patentable weight because the invention as claimed is drawn to a structure, not its intended use. Intended use and other types of functional language must result in a structural difference between the claimed invention and the

prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

On claims 24 and 29: the thickness of said polysilicon layer of said landing pad is in a range that substantially overlaps the range as claimed of about 100-400 angstrom, namely: between 300 and 1000 angstrom (col. 4, l. 31-33).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. ***Claim 23*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts (6,271,073 B1) in view of Parekh et al (6,331,720 B1).

Roberts teaches:

a substrate 112 (see Figures 3 and 4; and col. 3, l. 58-60),

a transistor (p-channel transistor, see col. 34, l. 36 and Figures 3 and 4) disposed on the substrate, comprising a gate layer 140 (with sub-layers 116 and 120; Figures 3F and 4; and col. 5, l. 49) and comprising a first doped region and a second doped region (right-most and central regions 124, being the source and drain regions of said transistor: see Figures 3 and 4; and see col. 4, l. 22-24) (N.B.: although said regions have the same numeral they are clearly distinct regions as otherwise the transistor would not be operative);

an inner landing pad 130 (col. 4, l. 31 and Figures 3 and 4), disposed on the first doped region and parts of the transistor (gate layer 140 and gate insulating layer, e.g.), comprising a polysilicon layer (col. 4, l. 35-38, and Figures 3 and 4);

a passivation layer 128/134/143 (col. 4, l. 28 – col. 5, l. 4 and Figures 3 and 4) formed on the inner landing pad (Figure 4) (N.B.: layers 128, 134 and 143 form a single laminate as they abut each other, and are all oxides, hence can be considered as an oxide layer), formed on the inner landing pad, the transistor, and the substrate (Figures 3 and 4), wherein the passivation layer is in contact with the second doped region 124 (Figures 3 and 4);

a second insulating layer 144 (col. 4, l. 65 – col. 5, l. 4 and Figure 4) comprising doped materials (being a BPSG layer; loc.cit.), disposed on the passivation layer, having a flat surface on the passivation layer (see Figure 4);

a contact plug 146 (col. 4, l. 65 – col. 5, l. 5), disposed on the second insulating layer and the passivation, electrically connecting with the inner landing pad 130; and

an interconnected landing pad 148, deposited on the contact plug.

By virtue of its material composition and laminate form the passivation layer has the capability to serves as a diffusion barrier because oxides are massive obstacles materially and are insulating, thus inhibiting diffusion. The limitation "serving as a diffusion barrier" indicates intended function or use. Intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Roberts does not necessarily teach the limitation that the gate layer 140 is "covered by a first insulating layer". However, it would have been obvious to include said limitation in view of Parekh et al, who, in a patent on an integrated circuit with field effect transistor and electrical contacts to the substrate, hence analogous art, teach a cap layer 17 of insulating material covering the gate layer 16 (Figures 1 and 8; and col. 5, l. 8-26) so as to protect the gate col. 5, l. 25-26). *Motivation* to include the teaching by Parekh et al in the invention by Roberts derives from the teaching by Parekh et al (loc.cit.) of the protective function of said insulating layer 17. Furthermore, additional obviousness derives from the consideration that the improvement through said protective insulating layer of gate layers in the art of integrated circuits with field effect transistors and passive electrical contact to the substrate was known and was part of the ordinary skill in the art as witnessed by Parekh et al.

3. ***Claim 24*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts and Parekh et al as applied to claim 23 above, and further in view of Hsu et al (6,221,767 B1).

As detailed, claim 23 is unpatentable over Roberts in view of Parekh et al. Neither Roberts nor Parekh et al teach the further limitation of claim 24 on thickness of the landing pad.

However, said range would have been obvious in view of Hsu et al, who, in a patent on the fabrication of a landing pad for integrated semiconductor circuitry including field effect transistors and contacts with the substrate (see "Background of the Invention", col. 1, l. 5-60, title and abstract), hence analogous art, teach the thickness of the inner landing pad to be between about 250 to about 400 angstrom (col. 3, l. 51-55), which overlaps with the range as claimed.

A *prima facie* case of obviousness typically exists when the ranges overlap the ranges disclosed in the prior art or when the ranges do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. See MPEP 2144.05.

4. ***Claim 28*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts (6,271,073 B1) in view of Parekh et al (6,331,720 B1).

Roberts teaches:

a substrate 112 (see Figures 3 and 4; and col. 3, l. 58-60),

a transistor (p-channel transistor, see col. 34, l. 36 and Figures 3 and 4) disposed on the substrate, comprising a gate layer 140 (with sub-layers 116 and 120; Figures

3F and 4; and col. 5, l. 49) and comprising a first doped region and a second doped region (right-most and central regions 124, being the source and drain regions of said transistor: see Figures 3 and 4; and see col. 4, l. 22-24) (N.B.: although said regions have the same numeral they are clearly distinct regions as otherwise the transistor would not be operative);

an inner landing pad 130 (col. 4, l. 31 and Figures 3 and 4), disposed on the first doped region and parts of the transistor (gate layer 140 and gate insulating layer, e.g.);

a passivation layer 128/134/143 (col. 4, l. 28 – col. 5, l. 4 and Figures 3 and 4) formed on the inner landing pad (Figure 4) (N.B.: layers 128, 134 and 143 form a single laminate as they abut each other, and are all oxides, hence can be considered as an oxide layer), formed on the inner landing pad, the transistor, and the substrate (Figures 3 and 4), wherein the passivation layer is in contact with the second doped region 124 (Figures 3 and 4);

a second insulating layer 144 (col. 4, l. 65 – col. 5, l. 4 and Figure 4) disposed on the passivation layer, having a flat surface on the passivation layer (see Figure 4);

a contact plug 146 (col. 4, l. 65 – col. 5, l. 5), disposed on the second insulating layer and the passivation, electrically connecting with the inner landing pad 130; and

an interconnected landing pad 148, deposited on the contact plug.

Roberts does not necessarily teach the limitation that the gate layer 140 is "covered by a first insulating layer".

However, it would have been obvious to include said limitation in view of Parekh et al, who, in a patent on an integrated circuit with field effect transistor and electrical contacts to the substrate, hence analogous art, teach a cap layer 17 of insulating material covering the gate layer 16 (Figures 1 and 8; and col. 5, l. 8-26) so as to protect the gate col. 5, l. 25-26).

Motivation to include the teaching by Parekh et al in the invention by Roberts derives from the teaching by Parekh et al (loc.cit.) of the protective function of said insulating layer 17.

Furthermore, additional obviousness derives from the consideration that the improvement through said protective insulating layer of gate layers in the art of integrated circuits with field effect transistors and passive electrical contact to the substrate was known and was part of the ordinary skill in the art as witnessed by Parekh et al.

5. ***Claim 29*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts and Parekh et al as applied to claim 23 above, and further in view of Hsu et al (6,221,767 B1).

As detailed, claim 28 is unpatentable over Roberts in view of Parekh et al. Neither Roberts nor Parekh et al teach the further limitation of claim 29 on thickness of the landing pad.

However, said range would have been obvious in view of Hsu et al, who, in a patent on the fabrication of a landing pad for integrated semiconductor circuitry including field effect transistors and contacts with the substrate (see "Background of the Invention",

col. 1, l. 5-60, title and abstract), hence analogous art, teach the thickness of the inner landing pad to be between about 250 to about 400 angstrom (col. 3, l. 51-55), which overlaps with the range as claimed. A *prima facie* case of obviousness typically exists when the ranges overlap the ranges disclosed in the prior art or when the ranges do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. See MPEP 2144.05.

6. ***Claims 25 and 30*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (5,895,961) in view of Xia et al (6,261,975).

As detailed above, claims 23 and 28 are anticipated by Chen. Chen does not necessarily teach the further limitations by either claim 25 or claim 30. *However, it would have been obvious to employ a silicon nitride support layer equivalent to layer 26 in Chen* used as conformal underlayer for the deposition of BPSG for planarization employing reflow (col. 4, l. 50-55) in a patent pertinent to said process (see title and abstract), because they teach that a FBPSG layer for planarization or reflow can be deposited on a silicon oxide underlayer but also on a silicon nitride underlayer (col. 7, l. 3-27). Applicant is reminded that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. See MPEP 2144.07.

7. ***Claims 26 and 31*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (5,895,961) and Xia et al (6,261,975) as applied to claims 25 and 30, respectively, above, and further in view of Lee (4,986,879).

As detailed above, claims 25 and 30 are unpatentable over Chen in view of Xia et al. Neither Chen nor Xia et al necessarily teach the further limitations of either claim 26 or claim 31.

However, conformal silicon nitride layers of Lee, who teaches that conformal silicon nitride layers can be reliably be made as thin as between 100 and 130 angstrom (see col. 1, "Brief Summary", lines 15-48). It would further have been obvious to manufacture said conformal underlayer as thin as possible in view of its contact function and also to save time and effort. Obviousness also flows from the consideration that a person of ordinary skill in the art has good reason to pursue the known options (thickness and material constitution of conformal underlayers for planarization and reflow) within his or her technical grasp. If this leads to the anticipated success, then this is likely the product not of innovation but of ordinary skill and common sense.

Response to Arguments

Applicant's arguments filed in Remarks of 7/9/07 have been fully considered but they are not persuasive. Although through substantial amendment to the previously pending claims 23-26 the new matter rejection has been overcome, the newly amended claims as well as the newly added claims are found partly anticipated and partly unpatentable over the prior art, as explained in the rejections under 35 U.S.C. 102(b) and 35 U.S.C. 103(a) overleaf, which are herewith included by reference in response to Remarks.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
September 14, 2007

Primary Patent Examiner:
Johannes Mondt (TC3600, Art Unit: 3663)